CLAIMS

What is claimed is:

1. A system for implementing vertical threading in a processor, comprising:
a header block that receives a multi-function signal and generates a plurality of signals using the multi-function signal; and
a data storage block that is responsive to the plurality of signals generated by the header block.

2. The system of claim 1, wherein the header block comprises header circuitry which distinguishes between different functionalities exhibited by the multi-function signal.

3. The system of claim 1, wherein the multi-function signal comprises a scan enable function, a clock enable function, and a clock disable function.

4. The system of claim 1, wherein the header block receives signals in addition to the multi-function signal.

5. The system of claim 4, wherein the additional signals received by the header block comprise a clock input signal and a global thread identifier signal.

6. The system of claim 5, wherein the global thread identifier signal is used by the processor to selectively indicate to the header block that the data storage block needs to switch process threads.

7. The system of claim 5, wherein the clock input signal is generated by the processor and is used by the header block to determine time references for operations in the header block.

8. The system of claim 1, wherein the plurality of signals generated by the header block comprise an external pulse signal, an inverted external pulse signal, a scan clock signal, and a local thread identifier signal.

9. The system of claim 8, wherein the external pulse signal is used by the data storage block as a time reference for operations in a normal mode.

10. The system of claim 8, wherein the inverted external pulse signal is an inverse of the external pulse signal, and wherein the inverted external pulse signal is used by the data storage block to facilitate operations in a normal mode.

11. The system of claim 8, wherein the scan clock signal is used by the data storage block as a time reference for operations in a scan mode.

12. The system of claim 8, wherein the local thread identifier signal is generated by the header block using a global thread identifier signal.

13. The system of claim 1, wherein the data storage block receives the plurality of signals generated by the header block, and wherein the header block and the data storage block are part of a multiple-bit flip-flop, and wherein the multiple-bit flip-flop is used in a processor pipeline.

14. The system of claim 13, wherein the processor pipeline comprises a plurality of multiple-bit flip-flops.

15. The system of claim 1, wherein the data storage block comprises at least one data storage element that is capable of storing data for a plurality of process threads.

16. The system of claim 1, wherein the header block controls a plurality of modes in which the data storage block may operate, and wherein the multi-function signal comprises additional functions.

17. A method for implementing vertical threading, comprising:
receiving a multi-function signal in a header block;
determining which function the multi-function signal serves;
generating signals within and from the header block according to the determination; and
operating a multiple-bit flip-flop in one of a plurality of operation modes dependent upon the determination of which function the multi-function signal serves.

18. The method of claim 17, wherein the multi-function signal can serve as a scan enable function, a clock enable function, and a clock disable function.

19. The method of claim 17, wherein the signals generated from the header block are received by a data storage block.

20. The method of claim 19, wherein the data storage block operates in one of the plurality of operation modes dependent upon the signals generated from the header block.

21. The method of claim 17, wherein the determination of which mode to operate the multiple-bit flip-flop comprises:

distinguishing between multiple characteristics of the multi-function signal;

using the multi-function signal to generate intermediary signals; and

using the intermediary signals to determine when the multiple-bit flip-flop should go into or remain in one of the plurality of operation modes.

22. The method of claim 21, wherein the intermediary signals are internal to the header block, and wherein the plurality of operation modes comprise a normal mode and a scan mode.

23. The method of claim 18, wherein the determination that the multi-function signal serves as the scan enable function indicates that the multiple-bit flip-flop should operate in a scan mode, and wherein the determination that the multi-function signal serves as the clock enable function indicates that the multiple-bit flip-flop should operate in a normal mode.

24. The method of claim 18, wherein the determination that the multi-function signal serves as the clock disable function indicates that the multiple-bit flip-flop should temporarily suspend normal mode data operations for alignment purposes.

25. The method of claim 17, further comprising:

inputting a first clock signal;

inputting the multi-function signal;

inputting a global thread identifier signal; and

selectively generating an external pulse signal, a scan clock signal, and a local thread identifier signal dependent upon the behavior of the pulse signal, the multi-function signal, and the global thread identifier signal.

26. The method of claim 25, further comprising:

generating an internal pulse signal using the first clock signal; and

using the internal pulse signal to activate the external pulse signal when the multi-function signal serves as a clock enable function.

27. The method of claim 25, further comprising:

deactivating the external pulse signal when the multi-function signal begins to serve as a scan enable function.

28. The method of claim 25, further comprising:

activating the external pulse signal at an end of a clock cycle in which the multi-function signal begins to serve as a scan enable function when the multi-function signal begins to serve as a clock enable function before the end of the clock cycle.

29. The method of claim 25, further comprising:

deactivating the external pulse signal when the multi-function signal serves as a scan enable function for more than one clock cycle.

30. The method of claim 27, wherein the multiple-bit flip-flop operates in a scan mode when the multi-function signal serves as the scan enable function for more than one cycle.

31. The method of claim 30, further comprising:
activating the scan clock signal when the multiple-bit flip flop is in the scan mode.

32. The method of claim 25, further comprising:
deactivating the external pulse signal when the global thread identifier signal toggles;
selectively generating the local thread identifier signal when the global thread identifier signal toggles; and
activating the external pulse signal at an end of a clock cycle in which the global thread identifier signal toggled.

33. The method of claim 25, wherein the external pulse signal, the scan clock signal, and the local thread identifier signal are received by the data storage block, and wherein additional signals are selectively generated to the data storage block.

34. The method of claim 25, wherein the multiple-bit flip-flop operates in a normal mode when the external pulse signal is activated.

35. The method of claim 17, further comprising:

converting an existing processor without vertical threading into a processor with vertical threading without changing an architectural layout of the existing processor.

36. An apparatus for implementing a vertical threading scheme, comprising:

means for inputting a clock signal;

means for inputting a multi-function signal;

means for inputting a global thread identifier signal;

means for distinguishing between different functionalities of the multi-function signal to determine which of a plurality of functions the multi-function serves; and

means for generating a plurality of signals based on the determination of which of the plurality of functions the multi-function serves, the clock signal, and the global thread identifier signal.

37. The apparatus of claim 36, wherein the plurality of signals comprises an external pulse signal, an inverted external pulse signal, a scan clock signal, and a local thread identifier signal.

38. The apparatus of claim 37, further comprising:

means for generating an internal pulse signal based on the behavior of the clock signal;

means for using the internal pulse signal as a time reference for operations;

means for using the internal pulse signal to generate the external pulse signal; and

means for using the internal pulse to generate the inverted external pulse signal.

39. The apparatus of claim 37, further comprising:

means for deactivating the external pulse signal when the global thread identifier signal toggles;

means for reactivating the external pulse signal at an end of a cycle in which the global thread identifier signal toggled; and

means for using the global thread identifier signal to generate the local thread identifier signal.

40. The apparatus of claim 37, further comprising:

means for deactivating the external pulse signal when the multi-function signal begins to serve as a scan enable function;

means for reactivating the external pulse signal dependent upon whether the multi-function signal stopped serving as a scan enable function before an end of a clock cycle in which the multi-function signal began serving as the scan enable function; and

means for activating a scan clock signal when the multi-function signal serves as the scan enable function for more than one clock cycle.

41. The apparatus of claim 36, further comprising:

means for activating an internal scan ready signal at a beginning of a clock cycle immediately following a previous clock cycle in which the multi-function signal began serving as a scan enable function; and

means for deactivating the internal scan ready signal when the multi-function signal stops serving as the scan enable function.